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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,768	03/15/2004	G. Glenn Henry	CNTR.2070	2645

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EXAMINER	
JUNG, DAVID YIUK	

ART UNIT	PAPER NUMBER
2134	

NOTIFICATION DATE	DELIVERY MODE
06/19/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTO@HUFFMANLAW.NET

Office Action Summary	Application No.	Applicant(s)	
	10/800,768	HENRY ET AL.	
	Examiner	Art Unit	
	David Y. Jung	2134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) 1-29 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 1-29 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 2004,2005,2007.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

CLAIMS PRESENTED

Claims 1-29 are presented.

CLAIM REJECTIONS

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Qi (cited by Applicant, EPO document, EP1215842) and Ulmann (cited by Applicant, ULMANN, B. "Designing a NICE Processor," Microprocessors and MIcrosystems, IPC Business Press LTD. London, GB. Vol. 23, No. 5. 25 October 1999. Pages 257-264. XP004321479 ISSN: 0141-9331) and Lynch (US Patent 5828873).

Regarding claim 1, Qi teaches "An apparatus for performing cryptographic operations, comprising: a cryptographic instruction, received by a [ ] as part of an instruction flow executing on said [ ], wherein said cryptographic instruction prescribes one of the cryptographic operations ... text ... (abstract: i.e., cryptographic processing, e.g., two level multiplexor)."

Qi is not explicit about other features of claim 1.

Ulmann teaches "computing device (section 1: i.e., processor)" for the motivation of escaping the typical flaws and drawbacks of other processors (section 1). Thus, Ulmann teaches to make a processor that can handle simplified operations such as described in Qi (the other reference). The hardware implementation, as broadly noted at abstract and detailed at other sections of Ulmann, is also noted.

Ulmann and Qi are not explicit about the other features of claim 1.

Lynch teaches "translation logic, operatively coupled to said [ ] instruction, configured to translate said [ ] instruction into micro instructions, wherein said micro instructions are ordered to direct said computing device to load a second input [ ] block and to execute said one of the [ ] operations on said second input [ ] block prior to directing said [ ] to store an output [ ] block corresponding to a first input [ ] block; whereby said output [ ] block is stored during execution of said one of the [ ] operations on said second input [ ] block (column 3, line 52 to column 4, line 17; figure 3, load/store unit 26; i.e., the loading and storing processes used when using load/store unit 26)" for the motivation of executing more without slowing down the processor (column 2, lines 21-37). As noted by Applicant in the specification of this application (such as at pages 1-19), much of the concepts of the floating point processing (as detailed in Lynch) are readily applicable to the cryptography processing (as recited in the claim).

Hence, it would have been obvious to those of ordinary skill in the art at the time of the claimed invention to combine the respective teachings of Qi, Ulmann, and Lynch

for the motivation noted in the previous paragraphs so as to teach the claimed invention.

Claims 1, 17, 24 are the independent claims.

Regarding claim 17, Qi teaches "... cryptographic ... text ... (abstract: i.e., cryptographic processing, e.g., two level multiplexor)."

Qi is not explicit about other features of claim 17.

Ulmann teaches "An apparatus for performing [ ] operations, comprising: translation logic, configured to translate a [ ] instruction into a sequence of micro instructions, said sequence of micro instructions (section 1: i.e., processor)" for the motivation of escaping the typical flaws and drawbacks of other processors (section 1). Thus, Ulmann teaches to make a processor that can handle simplified operations such as described in Qi (the other reference). The hardware implementation, as broadly noted at abstract and detailed at other sections of Ulmann, is also noted.

Ulmann and Qi are not explicit about the other features of claim 17.

Lynch teaches "a first micro instruction, directing that a second input [ ] block be loaded and that one of the [ ] operations be executed on said second input [ ] block; and a second micro instruction, directing that a first output [ ] block be stored, said first output [ ] block corresponding to a first input [ ] block upon which said one of the [ ] operations is executed; wherein said translation logic issues said first micro instruction prior to issuing said second micro instruction; whereby said output [ ] block is stored during execution of said one of the [ ] operations on said second input [ ] block (column 3, line 52 to column 4, line 17; figure 3, load/store unit 26; i.e., the loading and storing

processes used when using load/store unit 26)" for the motivation of executing more without slowing down the processor (column 2, lines 21-37). As noted by Applicant in the specification of this application (such as at pages 1-19), much of the concepts of the floating point processing (as detailed in Lynch) are readily applicable to the cryptography processing (as recited in the claim).

Hence, it would have been obvious to those of ordinary skill in the art at the time of the claimed invention to combine the respective teachings of Qi, Ulmann, and Lynch for the motivation noted in the previous paragraphs so as to teach the claimed invention.

Regarding claim 24, Qi teaches "A method for performing cryptographic operations in a device, the method comprising: ... text ... (abstract: i.e., cryptographic processing, e.g., two level multiplexor)."

Qi is not explicit about other features of claim 24.

Ulmann teaches "translating (section 1: i.e., processor)" for the motivation of escaping the typical flaws and drawbacks of other processors (section 1). Thus, Ulmann teaches to make a processor that can handle simplified operations such as described in Qi (the other reference). The hardware implementation, as broadly noted at abstract and detailed at other sections of Ulmann, is also noted.

Ulmann and Qi are not explicit about the other features of claim 24.

Lynch teaches "translating a [ ] instruction that prescribes execution of one of the [ ] operations into a first micro instruction and a second micro instruction, the first micro instruction directing the device to load a second input [ ] block be loaded and to execute

the one of the [ ] operations on the second input [ ] block, the second micro instruction directing the device to store a first output [ ] block, where the first output [ ] block correspond to a first input [ ] block upon which said the of the [ ] operations is executed; and issuing the first micro instruction to a cryptography unit prior to issuing the second micro instruction to the cryptography unit; whereby said issuing causes the output [ ] block to be stored during execution of the one of the [ ] operations on the second input [ ] block (column 3, line 52 to column 4, line 17; figure 3, load/store unit 26; i.e., the loading and storing processes used when using load/store unit 26)" for the motivation of executing more without slowing down the processor (column 2, lines 21-37). As noted by Applicant in the specification of this application (such as at pages 1-19), much of the concepts of the floating point processing (as detailed in Lynch) are readily applicable to the cryptography processing (as recited in the claim).

Hence, it would have been obvious to those of ordinary skill in the art at the time of the claimed invention to combine the respective teachings of Qi, Ulmann, and Lynch for the motivation noted in the previous paragraphs so as to teach the claimed invention.

Regarding claims 2-16, 18-23, 25-29, note:

Claims 2-3, 5, 18-19, 20, 25, 26, 27 (encryption, decryption, etc.) : such features are well known in the art for the purpose of cryptography.

Claims 4, 7, 22, 25, 26, 27, 29 (second block, 2-stage): this is the type of queuing (more than one stage, more than one block) that is the focus of Lynch. See the cited passages of Lynch.

Claims 6, 21, 28 (AES): such features are well known in the art for the purpose of cryptography.

Claims 8 (load/store micro instruction), Claim 9, 23 (x86 instruction format): this is the type of microcode handling that is the focus of Lynch. See the cited passages of Lynch.

Claims 10-16 (registers): such registers are well known in the art for the purpose of actuating a processor.

Conclusion

The art made of record and not relied upon is considered pertinent to applicant's disclosure. The art disclosed general background.

Points of Contact

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(571) 273-8300, (for formal communications intended for entry)

Or:

(571) 273-3836 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Jung whose telephone number is (571) 272-3836 or Kambiz Zand whose telephone number is (272) 272-3811.

David Jung

Patent Examiner

5/31/07